Design, synthesis and implementation of 8-bit accumulator using FPGA Board

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ABSTRACT

Accumulators are frequently used in digital circuits to store and process bi-nary data. The functionality of the accumulator is identical to a counter. In-stead of incrementing the counter value by a constant, the accumulator adds the input value to the current value. Using Verilog programming, an 8-bit accumulator was designed. In this work, to implement an 8-bit accumulator including functions: multiplication, division, and modulus. From the conducted simulation, the operations of 8-bit accumulator performs different operations based on different modes of operations along with displaying the results on FPGA. The Verilog HDL is used to design and simulate accumulator on Xilinx Vivado and generated bitstream files are uploaded to Nexys-4 Artix-7 FPGA board to show the result through the built-in seven-segment display. A Verilog top module is used to map the inputs parameters to the available onboard switches and push buttons to perform different operations and saving the results on accumulator. The internal clock of the board is 450 MHz and reduced to 10 Hz for an 8-bit accumulator and 10kHz for a seven-segment display using a clock divider.

KEYWORDS

accumulator, clock, seven-segment display, clock divider, addition, multiplication, division, modulus, Vivado

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1 INTRODUCTION

Nowadays, the field of electronics encompasses a vast array of technologies. Electronics is a physics and electrical engineering subfield concerned with emission, behavior, and effects. Electronics research has led to many developments in devices such as transistors, integrated circuits, lasers, and optical fibers. Those developments may have made it possible for mass production to supply all the electronic consumers. Indeed, the world is undergoing an electronic revolution that is at least as significant as the industrial revolution. These days the microprocessor is the central component of a computer system that executes arithmetic and logic operations, such as addition, subtraction, number transfer, and number comparison [1-2]. It is commonly referred to as a processor, central processing unit, or logic chip. These are used to store operands and results during program execution. Moreover, microprocessors differ in the internal storage provided by CPU data registers. The ALU will automatically load the result of a processing operation into the accumulator register of the vast majority of processors. Numerous modern microprocessors have an increased number of CPU data registers that can function as accumulators in complex arithmetic and logic operations. Accumulator-based microprocessors contain an accumulator register that participates in most of their internal processes. Consequently, most instructions in the instruction set pertain to the accumulator. The accumulator is an 8-bit register (which can store 8-bit data) part of the logical and ALU. The result of mathematical or logical operations is stored in the accumulator. Register A is also defined as an accumulator. Moreover, using the Nexys 4 Artix 7 board is a complete board with a ready-to-use digital circuit development platform [3-6]. This operates with its large or high-capacity FPGA, generous external memory USB, Ethernet, and other ports; the Nexys 4 can host designs ranging from introductory combinational circuits to powerful embedded processors. In this work, the simulation results will appear on the 7-segment display. Such design and analysis are helpful in creating a soft IP with addition of secured architecture design to make design less prone to hardware attack or IP theft challenges [7-12]. Addition security layer is hardware overhead per unit IC area but are now going popular in such design level implementations.

Fig. 1 shows the block diagram of the top module of the 8-bit accumulator that displays the results on a seven-segment display using Nexys 4 Artix 7 FPGA board. This includes the different blocks of the modules for the 8-bit accumulator, counter clock generator, Binary to BCD, refresh clock generator, and the seven-segment controller. The output ports are cathode and anode. It is observed that the input frequency of the clock is 450 MHz; however, when it is passed to the counter clock generator and refresh clock regenerator, the output frequency will be 10 Hz and 10 kHz, respectively. The clock has a 450 MHz clock input to the counter clock generator, binary to BCD converter, and refresh clock generator. The 10 Hz counter clock output is one of the inputs in the 8-bit accumulator, together with the 8-bit switch input, add, multiply, div, mod, and a reset. The 8-bit binary accumulator output value is the input of the binary to BCD control to have a binary coded decimal be displayed and pass its corresponding digit value in the seven-segment display. The result of the seven-segment controller is an 8-bit cathode and

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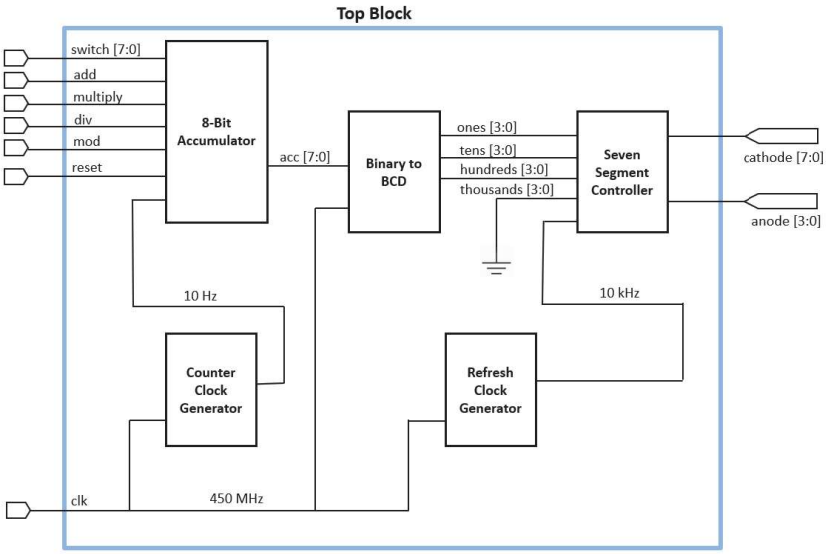

Figure 1: Top Block of an 8-bit Accumulator

a 4-bit-anode. The created program for the 8-bit accumulator functions to store the result of the chosen four mathematical operations, including addition, multiplication, division, and modulus operation in the accumulator [16-25].

To implement an 8-bit accumulator in a seven-segment display, a seven-segment controller is important. In connection to this, Figure 2 shows the block diagram that made up the seven-segment controller top module. The refresh counter module takes input from a system clock and gives a 2-bit vector output refresh counter to determine which digit will be displayed and which anode will be active. The anode control module takes the input vector refresh counter and switches on the anode accordingly. On the other hand, the BCD control module takes the input vector refresh counter and all four digits, which are the ones, tens, hundreds, and thousands. The output of the BCD control is a single digit that is to be shown according to the refresh counter value. The anode output and digit would be for the same 7-segment display. Lastly, the BCD to Cathode converter module inputs the binary data from the BCD control module and outputs the signals for the segments of the seven-segment display to show correct numbers on the seven-segment display.

2 VERILOG DESIGN MODULES

This section shows the Verilog code module for every block used in the block diagram shown in fig. 1 and 2. The Verilog code module includes the module for clock divider, BCD control, refresh counter, BCD to cathode, anode control, main design module and top module where mail design module and top module is described as:

2.1 *Main Module for 8-bit Accumulator*

```
module acc_8bit(in, add, multiply, mod, div, counter_clock_signal,
reset, acc);
input wire [7:0] in;
input wire counter_clock_signal;
input wire reset;
input wire add, multiply, mod, div;
output reg [7:0] acc = 0;
always@(posedge counter_clock_signal) begin
if(reset==1) acc <= 0;
else if(reset==0 && add==1 && multiply==0 && mod==0 &&
div==0) acc <= acc + in;
else if(reset==0 && add==0 && multiply==1 && mod==0 &&
div==0) acc <= acc * in;
else if(reset==0 && add==0 && multiply==0 && mod==0 &&
div==1) acc <= acc / in;
else if(reset==0 && add==0 && multiply==0 && mod==1 &&
div==0) acc <= acc % in;
else acc <= acc;
end
endmodule
```

2.2 *Top Module*

```
//Top Module
module acc_top(clk,switch,reset,add,multiply,mod,div,anode,cath-
ode);
input wire clk;
input wire [7:0]switch;
input wire reset, add, multiply, mod, div;
output wire [3:0] anode;
output wire [7:0] cathode;
wire refresh_clk;
wire counter_clock_signal;
wire [7:0] eight_bit_acc_value;
wire [3:0] ones;
wire [3:0] tens;
wire [3:0] hundreds;
```

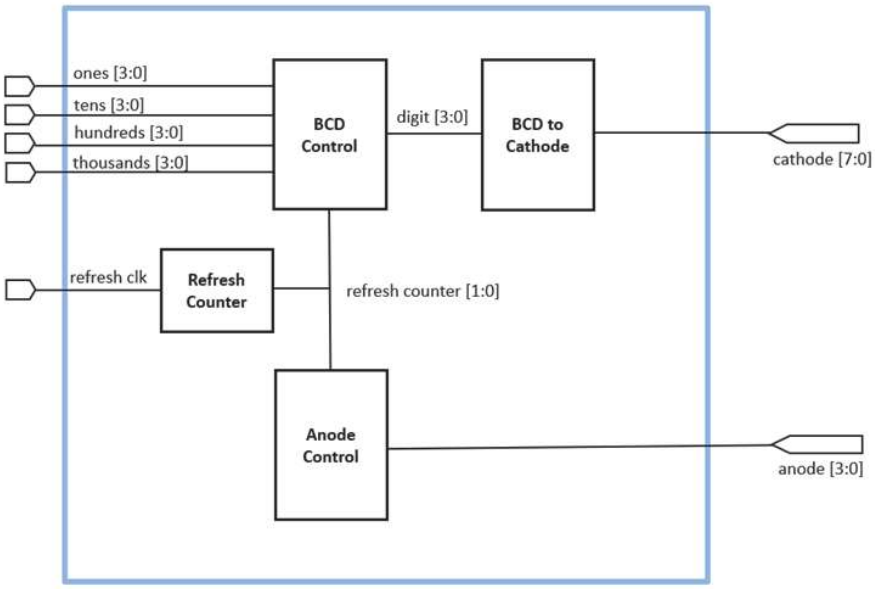

Figure 2: Seven Segment Controller

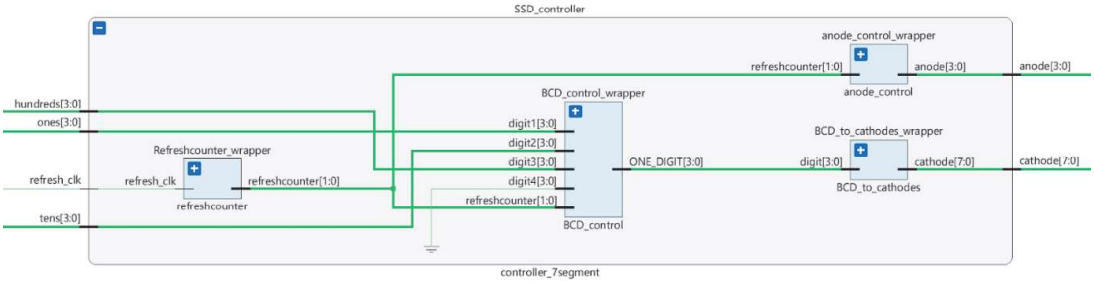

Figure 3: RTL Schematic Diagram

clock_divider #(4999) refreshclock_generator(clk,refresh_clk); //10kHz clock signal
clock_divider #(4999999) counterclock_generator(clk,counter_clock_signal);
acc_8bit accumulator(switch, add, multiply, mod, div, counter_clock_signal, reset, eight_bit_acc_value);
binary_to_BCD Convert_Binary_to_BCD (clk, eight_bit_acc_value,ones,tens,hundreds);
controller_7segment SSD_controller(refresh_clk,ones,tens,hundreds,anode,cathode);
endmodule

3 RESULT AND DISCUSSION

The Verilog module test bench results along with synthesis and results are obtained with Xilinx Vivado on FPGA boards.Dealy and power analysis is carried for typical PVT values.

3.1 *RTL Schematic*

Fig. 3 shows the block diagram of the top module of the 8-bit accumulator that displays the results on a seven-segment display using Nexys 4 Artix 7 FPGA board. It satisfies the requirement for the block diagram. The first image includes counterclock_generator, accumulator, Binary_to_BCD Converter, and refreshclock_generator. The second image shows the details for the Seven Segment Controller, where several more parts are added, such as refresh counter, BCD control, anode control, BCD_to_Cathode, and the output anode and cathode.

3.2 *Behavioral simulation waveform*

Fig. 4 shows the behavioral simulation of the 8-bit Accumulator by simulating the test bench of the Verilog code. It has four functions: add, multiply, div, and mod. These functions will only operate at positive edge transition. When “add” is high, the values in the

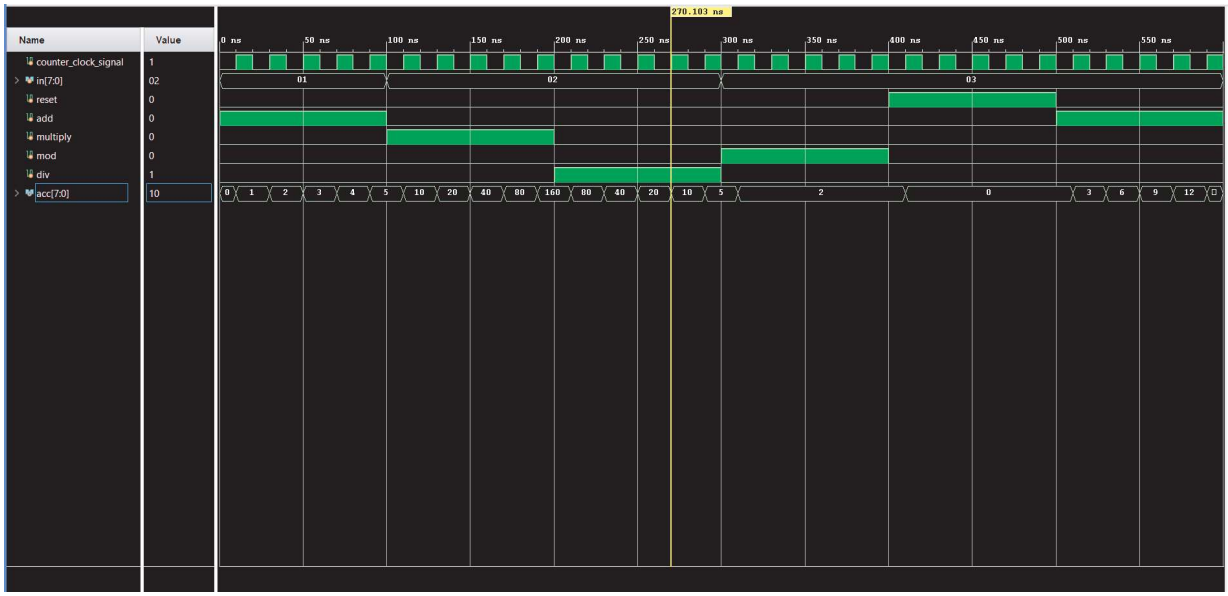

Figure 4: ***Behavioral Simulation of the 8-bit Accumulator***

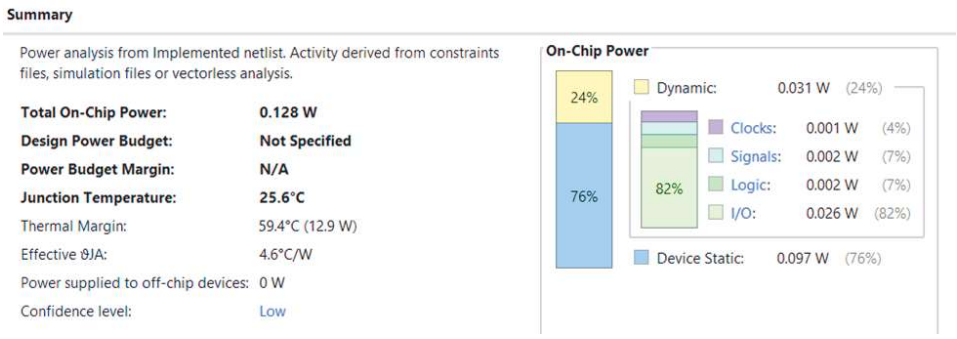

Figure 5: Power Analysis Summary

accumulator are added by 1. When "multiply" is high, the values in the accumulator are multiplied by 2. When "div" is high, the values in the accumulator are divided by 2. Lastly, when "mod" is high, it applies modulus to the value in the accumulator, wherein when the value is divided by 3, the remainder will be displayed. The values being used in this simulation are included in the testbench.

3.3 *Power & timing analysis report*

Fig. 5 shows the summary of the power analysis that has been obtained through the implementation netlist in Vivado. It is concluded that the dynamic power was 0.031 watts, equivalent to 24%, and the static power was 0.097 watts, equal to 76% of the total power. However, adding both powers will result in 0.128 watts of total on-chip power. It is noticeable that the static power was greater than the dynamic power because the system uses a clock. Based on the diagram, the junction temperature was 25.6 degrees Celsius. Fig. 6 shows the design timing summary. The worst negative slack (WNS) is 4.96 ns, the worst hold slack (WHS) is 0.147 ns, and the worst pulse width slack (WPWS) is 4.5 ns. The system meets all timing constraints. Further improvement in accumulator design is possible with optimized algorithms with addition of machine learning based design techniques [13-15]. Since accumulator is part of various computing blocks, so the delay and power associated to this should be optimized with exploration of new designs.

4 CONCLUSION

Accumulator is a sequential circuit since it uses the internal clock of the FPGA board. The output will be added, multiplied, divided, and operate modulus function continuously, depending on the operation used to the input every time the clock is in positive edge transition. The output of the accumulator is in the binary system, and a binary-to-BCD decoder was used to convert it to binary coded decimal (BCD), which is divided into ones, tens, hundreds, and thousands. The maximum output is 255 since the input is eight-bit, so "thousands" is connected to the ground. Using the BCD-to-seven-segment decoder, the digits in ones, tens, and hundreds can

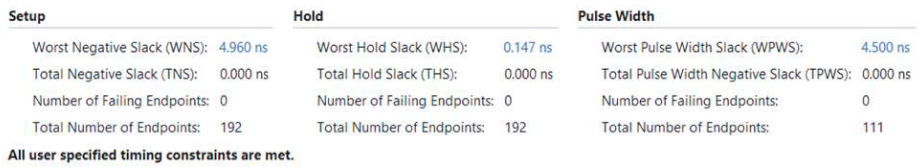

Figure 6: Design Timing Summary

be shown in the seven-segment display. Using an FPGA board, switches were used for the inputs of an accumulator, and buttons were used for changing operations and reset. Nexys-4 Artiz-7 FPGA board has an internal clock frequency of 450 MHz which is too fast for the human eye to see when the code is implemented on the board. A clock divider was used to decrease the clock frequency and monitor the FPGA board's output.

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